REMARKS

Claims 1-20 remain in the present application. Claims 1 and 10 are amended herein. Applicants respectfully assert that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections based on the arguments set forth below.

Claim Rejections – 35 U.S.C. §103

Claims 1-3, 6, 10-11 and 15-16

Claims 1-3, 6, 10-11 and 15-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent Number 5,994,937 to Hara et al. (hereafter referred to as "Hara"), in view of United States Patent Number 5,926,045 to Kwon (hereafter referred to as "Kwon"), and further in view of United States Patent Number 6,031,366 to Mitsuishi (hereafter referred to as "Mitsuishi"). Applicants have reviewed the cited references and respectfully assert that the embodiments of the present invention as recited in Claims 1-3, 6, 10-11 and 15-16 are not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1, which recites a timer circuit comprising (emphasis added):

> an output stage coupled to a configurable delay element, wherein said configurable delay element comprises a plurality of selectively-activated components operable to adjust a delay through said timer circuit, and wherein said output stage receives a signal generated by said configurable delay element; and
>
> a pull-down path coupled to said output stage and comprising a circuit for providing a selectable amount of pull down current, said pull-down path also coupled to receive a reference signal that varies in proportion to temperature and wherein said delay through said timer circuit is inversely proportional to said temperature.

Independent Claim 10 recites similar limitations to independent Claim 1. Claims 2-3, 6, 11 and 15-16 depend from their respective independent claims and recite further limitations to the claimed invention.

Applicants respectfully assert that Hara fails to teach or suggest the limitation of "wherein said output stage receives a signal generated by said configurable delay element" as recited in independent Claim 1. As recited and described in the present application, an output stage receives a signal generated by a configurable delay element.

In contrast to the claimed embodiments, Applicants understand Hara to teach that an output stage does not receive a signal from a delay circuit. For example, as shown in Figure 4 of Hara, elements 402 and 406 (cited on page 2 of the rejection as teaching the claimed configurable delay element) receives signals from transistors 410 and 412 (cited on page 2 of the rejection as teaching the claimed output stage). As such, Applicants respectfully assert that Hara teaches away from the claimed embodiments by teaching that a delay element receives a signal from an output stage instead of an output stage receiving a signal from a configurable delay element as claimed.

Applicants respectfully assert that both Kwon and/or Mitsuishi, either alone or in combination with Hara and/or one another, fail to cure the deficiencies of Hara discussed above with respect to independent Claim 1. Specifically, Applicants respectfully assert that Kwon and Mitsuishi also fail to teach or suggest the limitation of "wherein said output stage receives a signal generated by said configurable delay element" as recited in independent Claim 1.

Additionally, Applicants respectfully direct the Examiner to MPEP §2143 which states that one of the requirements for establishing a *prima facie* case of obviousness is showing "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Page 3 of the rejection states that the motivation for combining Hara and Mitsuishi is to save cost, but as discussed in the response to the previous Office Action with a mail date of 1/23/07, replacing Hara's transistors 414 and 424 with the current source taught in Figure 3 of Mitsuishi (e.g., adding a significant number of circuit elements as well as additional circuitry to control the switches) would *add significant cost* to Hara's circuit instead of reducing cost as suggested by the rejection. As such, assuming that the Examiner is relying upon knowledge generally available to one of ordinary skill in the art to show a suggestion or motivation to combine Hara and Mitsuishi in the claimed fashion, Applicants respectfully request that the Examiner provide documentary evidence supporting the alleged implicit suggestion/motivation (e.g., as suggested by MPEP §2144.03) or instead withdraw the rejection if such documentary evidence is not provided.

For these reasons, Applicants respectfully assert that independent Claim 1 is not rendered obvious by Hara in view of Kwon, and further in view of Mitsuishi, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since independent Claim 10 recites limitations similar to those discussed above with respect to independent Claim 1, independent Claim 10 also overcomes the 35 U.S.C. §103(a) rejections of record. Since Claims 2-3, 6, 11 and 15-16 recite further limitations to the invention claimed in their respective independent claims,

Claims 2-3, 6, 11 and 15-16 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 1-3, 6, 10-11 and 15-16 are allowable.

Claims 1-20

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hara in view of Kwon, further in view of Mitsuishi, and further in view of United States Patent Number 6,388,490 to Saeki (hereafter referred to as "Saeki"). Applicants have reviewed the cited references and respectfully assert that the embodiments of the present invention as recited in Claims 1-20 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki for the following reasons.

Applicants respectfully assert that both Saeki, either alone or in combination with Hara, Kwon and/or Mitsuishi, fail to cure the deficiencies of the Hara/Kwon/Mitsuishi combination discussed above with respect to independent Claim 1. Specifically, Applicants respectfully assert that Saeki also fail to teach or suggest the limitation of "wherein said output stage receives a signal generated by said configurable delay element" as recited in independent Claim 1.

Applicants respectfully direct the Examiner to independent Claim 17, which recites a method of varying a delay of a timer circuit comprising (emphasis added):

> during configuration of said timer circuit, setting a first plurality of configuration bits which control the amount of elements coupled to an output stage of said timer circuit to set an amount of delay through said timer circuit;
> during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage; and

during operation of said timer circuit, varying a reference signal coupled to said pull down path to vary delay though said timer circuit inversely proportional to temperature of said timer circuit.

Claims 18-20 depend from independent Claim 17 and recite further limitations to the claimed invention.

Applicants respectfully assert that Hara fails to teach or suggest the limitation of a "during said configuration, setting a second plurality of configuration bits which control an amount of pull down current through a pull down path of said timer circuit to set an amount of delay through said timer circuit, said pull down path coupled to said output stage" as recited in independent Claim 17. As recited and described in the present application, a configuration stage and operation stage of the timer circuit exist. During the configuration stage, configuration bits are set to control the delay through the timer circuit by determining an amount of elements coupled to the output stage of the timer circuit. Additionally, a second set of configuration bits are set during configuration to control an amount of pull-down current of the timer circuit.

In contrast to the claimed embodiments, Applicants respectfully assert that the cited Hara/Kwon/Mitsuishi/Saeki combination fails to teach or suggest setting a plurality of configuration bits to control pull down current *during configuration* (as opposed to during operation) as claimed. For example, even if Mitsuishi's switches and transistors as depicted in Figure 3 of Mitsuishi were added to Hara's circuit depicted in Figure 4 of Hara, neither reference teaches or suggests that adjustment of the switches are performed *during a configuration stage* as claimed. Moreover, Mitsuishi states that Mitsuishi's variable current source is used by a DAC circuit to generate analog signals from digital signals, and therefore, Mitsuishi teaches away form the claimed embodiments by

teaching a variable current source used *during operation* of a circuit instead of during configuration as claimed.

For these reasons, Applicants respectfully assert that independent Claims 1, 10 and 17 are not rendered obvious by Hara in view of Kwon, further in view of Mitsuishi, and further in view of Saeki, thereby overcoming the 35 U.S.C. §103(a) rejections of record. Since Claims 2-9, 11-16 and 18-20 recite further limitations to the invention claimed in their respective independent claims, Claims 2-9, 11-16 and 18-20 also overcome the 35 U.S.C. §103(a) rejections of record. Therefore, Claims 1-20 are allowable.

CONCLUSION

Applicants respectfully assert that Claims 1-20 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 9/14, 2007

BMF

Bryan M. Failing
Registration No. 57,974

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060